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Smart Semiconductor Testing Systems: Fusion of Embedded AI And Scalable Data Pipelines

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Abstract

Semiconductor companies are challenged by increasingly complex testing requirements coming from their customers and technology, as the design of modern System-on-Chips (SoCs) evolves into multi-chiplets. New AI-driven paradigms are needed to facilitate a massively parallel high-throughput test methodology while still allowing tight test channel characterization that affects both yield and performance of the complex designs. With the increase in chip complexity and design autonomy of third-party chiplets, a whole new add-on market for in-die and package-level testing is created, and access to the test systems is kept tightly.

A new architecture for the system under test (SUT) is presented based on decisions at test time and embedded intelligence combined with a distributed AI-based device that abstracts the test flow towards a Domain-Specific Language (DSL) API. This new approach is complemented by a novel design-to-test procedure and scalable machine learning pipelines on chiplet level. With this approach, a Semantic Web-based ecosystem of tools and libraries is created that links simulators and correlators and allows engineers to compose powerful packages of tasks, lab experiments, and production data mining. Traditional semiconductor integrated circuit (IC) test systems are fast reaching their limits with respect to both test data throughput in the order of petabytes and complexity of platform and device under test which need to be test parallelized in order to ensure operational use. For SoCs and their Subsystems, an architecture and implementation of a non-standard test methodology is proposed that is distributed, massively parallel, and AI driven. The ambition is to merge the fabrication test domain with various application domains in order to perform heterogeneous tests.

Keywords: Smart semiconductor testing, Embedded AI, Scalable data pipelines, AI-driven test automation, Semiconductor test analytics, Edge AI in testing, Real-time test optimization, Predictive maintenance, Machine learning in IC testing, Data-driven test systems, High-throughput testing, Adaptive test frameworks, Test data orchestration, Intelligent test strategies, Yield optimization.

1. Introduction

As electronics become an increasingly large part of everyday lives, the demand for smarter devices grows and raises the complexity of semiconductor products. Growth is driving the increasing challenge between the very high complexity of SoCs versus known good die (KGD) whose quality continues to degrade due to continuing geometrical and electrical scaling trends down to the nanometers. As a result, there is a need for smart testing systems that require fully automated, fast and scalable high-quality testing of hundreds of chips per hour.

Nevertheless, due to increasing complexity, traditional semiconductor testing is at its limits and hardware-per-second (HWP) is still a software factor-100 away from industrial needs. As a response to ever growing testing demands, the industry is starting its first steps towards massively parallel, hybrid analogue/digital, and distributed semiconductor testing. These hardware systems require fully automated testing and a cloud computing environment for development as well as production. As a response to ever growing testing demands, such modular and scalable test systems are required for the deployment of fault-detection methods based on state-of-the-art chip design tools as well as these new and expected smart enhancements. As many of these methods are implemented in the design phase of chips, smart semiconductor testing systems not only comprise modular hardware, data pipelines and cloud environments but also chip design support and ‘programming’ and control learning. Pre- and post-fusion testing rely on the data gathered during manufacturing. Thus far, chips have been tested separately, resulting in long runtimes and limited detection capabilities. The next step is to re-open the decision masks of these chips after assembly in 3D stacked dies. Types of data sets to be pooled and ways to combine them are conduction paths, input and response pins, and many others. To harvest this data, clustering and deep learning techniques are applied to yield prediction of the likelihood of a good or a bad die. This screening allows flagging chips/groups that contain too many bad dies. Furthermore, the ‘good’ decision masks are re-opened in versions that reduce runtime, but retain sensitivity. Since 90% of chip pins are for data input/output, even a low ratio of detection stuck-at malfunctions can lead to catastrophic failures. Thus, the response capture and compare (COM) approach is used: a number of simple vector pairs are applied to all chips whose results are equal (→passed) or different (→failed). Finally, a ‘trained’ software embedded in the tester also decides on the malfunctioning pin and applies signatures that can locate the fault to an area of the die thus limiting the very disruptive and long failure analysis.

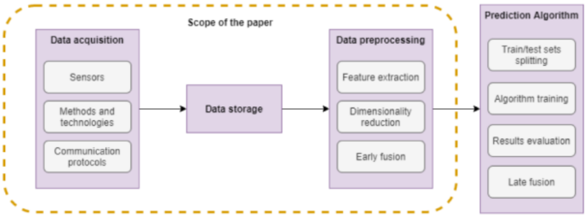

Fig 1: Smart Semiconductor Testing Systems

1.1. Background And Significance

Smart Testing Systems for Semiconductor Chips aim to maximize chip quality while minimizing waste. Intelligent test systems can lower overall maintenance costs and minimize human errors. Manufacturers can guarantee high product quality when adopting more advanced quality assurance methodologies with embedded AI chips integrated into scalable data pipelines of automated test equipment (ATE). Patterns that relate causes to chip performance can be detected from an ATE's built-in self-diagnostic data using deep learning models. Missed early warnings can be avoided using attention mechanisms. Algorithms can be trained to recognize key data-drivers from historical test data using self-supervised learning architectures for scalable performance prediction.

Statistical process monitoring can search for signals that deviate from normal behavior and identify potential performance issues and fault sources. Predictive chip quality assurance is achieved using random forest models that account for wafer and probe measurements. Detector calibration maps for standard digital cells can be generated using a semi-supervised learning model. As a prospective direction of research, methods for building and utilizing detectors for scanning flux on a chip can be investigated.

Real-time performance prediction can create a probabilistic map from recent performance tests with estimated overall device counts. Early warnings of process drifts can be provided with minimum extra runtime. Note that full device specifications from all guard band tests are available for chip validation, which spontaneously creates a known-case analysis scenario. The examination could lead to the growth of desired technology. An AI-PAT-like metabolic system can be constructed for prospective chip testing global service. On-line chip performance can be interpreted based on the internal architecture of shortened attention-augmented fine-tuning transformers, fed with test parameters assembled. Training processes and run-time malfunctions can be detected using sliced long-short-term memory models and isotonic regression. For maintained testing quality assurance, fast on-demand sensitivity bit mapping methods can be devised using vote-style ensemble learning.

This effort aims to explore prospective research opportunities and methods for lower-cost and higher-quality tests of semiconductor chips with a dedicated workshop. Specific attention is given to on-chip intelligent information extraction, training on-chip models from historical data and on-the-fly knowledge refinement, analyzing data from multiple semiconductor testing stages, and validation and auditing approaches of AI systems for semiconductor chips.

Equ : 1 Test Quality Function (TQF)

$$\mathrm{TQF} = \alpha \cdot A_{\mathrm{AI}} + \beta \cdot C_{\mathrm{test}} - \gamma \cdot T_{\mathrm{latency}}$$

- A_{AI}: AI model accuracy
- C_{test}: Test coverage
- T_{latency}: Inference + test pipeline latency
- α, β, γ: Weighting coefficients

2. Overview of Semiconductor Testing

The devices in which integrated circuits (ICs) are typically fabricated have specific electric properties. Following wafer fabrication, these properties are verified by testing the ICs in a form called "die." A die is a single IC that has been separated from the wafer. Testing in die form is less accurate since it is not in the form of package testing. However, die-level testing can be very fast and is therefore widely used testing methods by wafer fabrication plants and module assembly companies to weed out non-conforming ICs before they are packaged and taped for shipment, testing of packaged ICs is also performed by semi-automated equipment. After IC packages are loaded on a test board, the tester verifies the external pin parameters.

The functional testing of packaged ICs is performed either manually or by automated testing equipment (ATE). Manual testing can handle complexity, higher reliability, and throughput. Automated test equipment is used by high production-volume assemblers of standard devices. Most devices are tested at the die level before being packaged. Pin to die correspondence maps for each IC type being tested are stored in the tester. The IC's input/output (I/O) pins, which are connected to the tester, are also mapped to pins soldered or otherwise connected to a socket on which the IC package is mounted.

The tester must be configured to match each die and its ordered set of tests. In most ATE, the config selection is done interactively by dialing before test start. The large number and variety of devices being tested results in non-trivial handling and configuration costs. This includes test set-up time. Changes are often made in accordance with the updated performance goals set by marketing, or in view of recognizing tutorials for possible additional tests. New chips are in production risk in a few commodity types, fixed config machine designs complying with the subdivision of labor may be used.

3. Role of AI in Semiconductor Testing

The COVID-19 pandemic and subsequent semiconductor supply chain disruption highlighted the U.S. reliance on foreign semiconductor suppliers. In response, Congress enacted the CHIPS for America Act which authorizes $52 billion in grants and loans to construct, expand or modernize semiconductor facilities in the United States. The U.S. semiconductor industry has shifted focus to advanced packaging with an emphasis on Heterogeneous integration and using multiple die types in a single package. A combination of die types is preferred to reduce costs, improve performance, and provide new functionality.

For each packaging type, the chips go through a series of assembly steps to attach and protect the die combination in the package. In these packages, the dies are carefully positioned to attain high performance and reliability. As the number of die types increases, the impact of the processing steps becomes more pronounced. One area of concern is potential damage to the die during the Attack, Underfill, and Mold flow steps due to thermal, mechanical or chemical interactions. To assess the die quality, each die is tested before assembly. The best testing scenario would ensure the die functionality is thoroughly assessed and provide test impressions that allow for safety verification for the subsequent assembly and packaging steps.

Modern high-speed serial memories require specific and stringent voltage and timing iterations at the edge of voltage and timing. Each of the individual requirements can exceed the available ATE capabilities and therefore need to be measured separately. To make the measurements pass/fail a lot of post processing and analysis are required on the ATE and therefore the edge limitation is only monitored on the ATE input side.

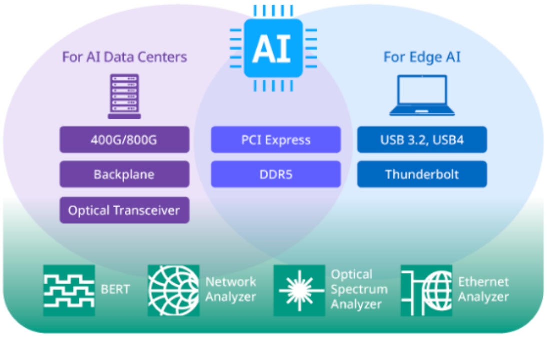

Fig 2: AI in Semiconductor Testing

3.1. Historical Context

The rapid advancements in semiconductor technology and an equally growing need to characterise, calibrate, and repair the ever-more complex devices have had significant implications for instrumentation and data analytics in semiconductor DC testing, timing-related on-chip signal integrity, ring-oscillator-based RF measurement, power integrity, and chip-level interconnect testing. This paper presents a broad overview of state-of-the-art research and development efforts in embedded AI schemes and large-scale data processing and machine-learning (ML) methods to transform semiconductor measurement systems into intelligent smart instrumentation and knowledge factories.

Semiconductor technology scaling is an essential driver for Moore’s Law, have boosted device complexity beyond one billion and, in semiconductor manufacturing, Fab infrastructures too have massively evolved from a handful of tools to 1000s of them. Nowadays, chips are often multi-dies with multiple chips fabricated onto a single die and chiplets, and multi-function systems on chip (SoCs), which can be as complex as supercomputers or human brains. Characterisation, calibration, and diagnosis of chips are more than ever complex, demanding a vast amount of characterisation, calibration, and diagnostic data for each die. Traditional data processing and management methods have reached their limits or have become too inefficient to address big data challenges. A large pool of raw measurement data is often not reused, simply stored and forgotten. The synergy of the four trends spurred a surge of interest in artificial intelligence (AI), which aims to mimic human intelligence and automate the workforce.

AI became known as the new “electricity” for every sector of life. AI-driven smart instrumentation has been intensively studied and developed emerging as a new commercial product for many industries. With the support of cloud computing, GPU, and automation of data processing flow, AI applications in measurement and data analytics in all conceivable areas are flourishing. Current state-of-the-art approaches include smart power integrity and data analytics/ML engines to aid power integrity measurement interpretation, smart SoC Drive Electronics for FTQ and data clustering, smart loading tests and covert calibration, and methodology for collecting chip-level test measurement data in the industry.

3.2. Current Applications

Smart Semiconductor Testing Systems (SSTS) is an amalgamation of algorithmic, architectural, and application-level innovations to explore the essential capabilities of embedded AI in handling elemental but complex operations in the semiconductor testing ecosystem intelligently. Gradual power reductions, size decreases, and increasing applications force products developed on scalable technologies. Scaling has significantly impacted the testing process in the semiconductor ecosystem, enabling tools with enhanced throughput and precision. But the number of samples has increased exponentially with the reduction in node capacitance. Each sample position represents the physical attributes of the underlying device, which could be a nanometer-scale transistor or a multiple mm scale power semiconductor module. It is myriads in tuples, enabling modes of separation of interest. Most common data analytics and interpretation methods are inefficient, lacking a priori extracted physics, evolving models, and edge statistics estimation. Embedded AI aims to fill this gap in the semiconductor testing ecosystem.

The integrated implementation of scalable and physically informed AI algorithms presently stands tall in challenges related to device characterization and reliability and can handle hundreds of millions of samples per measurement. Non-intrusive sampling and optimization paradigms can also transform inputs in space, time, and frequency domains into a favorable form for AI models in real time with power and area reductions. The choice of architecture impacts the performance and scalability of AI algorithms. Options include GPUs, FPGAs, RTPs, and application-specific designed circuits. Dedicated hardware implementations for saliency extraction, compression, and clustering are in production. Also ongoing is a chip for multi-dimensional data analysis that leverages sparsity in space, time, and trainability.

Many industries such as semiconductors face challenges with rapidly rising costs due to factors such as high wage economies and escalating demands for capacity due to soaring data production and storage needs. There are calls for urgent actions to be taken to address these challenges. Cloud-based data handling seems like Silicon Valley's answer. There is already an enormous battle underway for data turf and analytic algorithms. But any solution from silicon valley will ultimately be bottlenecked with an overwhelming bottleneck to sending and receiving data. For semiconductor testing, it is paramount to preserve the emission side measurements, grasp control information on test timings, transfer test stimulus and setup, and gather processed measurements on time to rerun the test. Running deep learning inference takes time and has to be replayed for the many sample chips of ASICs.

3.3. Future Trends

The future of semiconductor manufacturing and testing industries rests heavily on the shoulders of AI technology. Intelligent semiconductor testing, implementing cutting-edge AIs at each stage of the semiconductor manufacturing/test flow, is expected to drastically increase turnaround time (TAT) while improving accuracy. To fully unleash the capabilities of AIs in semiconductor testing, especially as SCI’s and sophisticated AIs grow bigger and more complex, it is critical to effectively integrate AIs, data, devices, systems, and processes. A data-focused approach is also presented as an essential avenue for the AI advancement. The data pipelines should be streamlined to continuously collect, navigate, analyze, and utilize data in the fastest and easiest manner possible.

Downstream component extraction, which identifies and extracts electrical elements fabricated inside a TEST chip, is one of the most crucial processes. It enables estimation of the electrical parameters necessary for in-depth physical failure analysis. A combination of data pipeline and embedding Machine Learning (ML) and Generative Adversarial Networks (GAN) revealed a viable solution to the problem. Fundamental concepts and challenges in establishing the data pipeline, screening, and assembling the chip test structure are described. Subsequently, generative and predictive models to produce training sets of chips and their component parameters are introduced together with augmentation methods. Two types of ML architectures to fuse the generative probabilities of multiple predictions/estimates or to ensemble different test structures, and to provide insights on the plausibility of detected components are proposed.

Test Data Management (TDM), the search, organization, analysis, and visualization of test, operational, and design data, are critical in semiconductor testing. MLOps is essential in TDM to ensure the efficiency of testing and continued growth of AI based testers and utilities. Global business issues resolved by MLOps such as reduction in test time, accuracy of test coverage, raw data sorting and efficient analysis are illustrated. Machine Learning (ML) capabilities embedded in semiconductor testers are introduced to significantly improve testing efficiency through enhanced automation, predictive test capability and smart analysis. Next lay out plans to implement MLOps, State of the Art (SOTA) test data tools, challenges in automating tests and organizing data are discussed. Finally, frameworks of transferable utilities across testing domains in Edge AI and memory testing, innovative visualizations to facilitate data guidelines and actionable insights, and TDM elements essential for a robust engineering device organization and retrieval system are presented.

4. Embedded AI Technologies

Embedded Artificial Intelligence (AEI) technology is a major leap in AI computing, and can provide real smartness in devices at a lower cost than the current remote smartness. The demand for smartness in embedded systems has been mounting in the past few years in various industries, such as consumer electronics, mobile devices, automotive applications and industrial automation. The buying decisions are more margin-sensitive, and more integrated functions are envisaged for better user experiences. Applications generally involve the on-par deployment of AI algorithms running forecasting and transformation at different frequencies. To cope with the demand for smartness from edge devices, many companies are developing AI chips for edge applications. These edge AI chips target low-power devices and sensors for triggering actions in a fast and safe manner.

Embedded smartness for AI chip implementations in devices is considered to function on the edge of the network and inside devices. Consequently, data acquisition needs to be conducted locally, and sensors are expected to become more intelligent in lieu of their high-accuracy imaginations. There have been notable works in implementing highly complex networks that can learn from raw pixel data and become more attention-grabbing than humans in intelligent surveillance systems, indicating the potential of edge smartness and the major AI system shift to raw signal processing.

Particularly challenging, but promising, constraints and priorities arise in the design fold of embedded AI implementations in devices at the edge of networks. These challenges and prior trends include greater interest in chip implementation, and the notion of raw signal processing at the edge, and demand for neural types of networks and explainable AI algorithms. On the other hand, data acquisition, design and processing methodologies for improved efficiency on low-cost devices should be investigated with the continuous development of AI technologies.

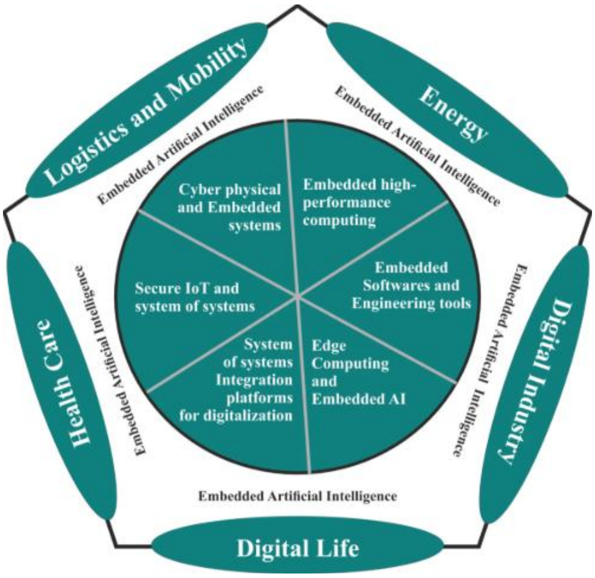
Logistics and Mobility
Energy
Digital Industry
Digital Life
Health Care
Embedded Artificial Intelligence
Embedded Artificial Intelligence
Embedded Artificial Intelligence
Embedded Artificial Intelligence
Embedded Artificial Intelligence
Cyber physical and Embedded systems
Embedded high-performance computing
Embedded Softwares and Engineering tools
Edge Computing and Embedded AI
System of systems Integration platforms for digitalization
Secure IoT and system of systems

Fig 3: Embedded Artificial Intelligence

4.1. Machine Learning Algorithms

This section summarizes various techniques using machine learning that enhance the functional testing process for a selected group of designs or instances. A variety of algorithms is employed in this section to cover a wide spectrum of application segments. This group shows applicability for various functional verification purposes.

The functional verification of processors has proved to become very complex. Several machine learning and data mining techniques are presented to automate processor verification. For a given golden model binary level description of the processor cores and the design under verification, the techniques extract the important state region of the system and logically partition it to integrate with the formal verification tool.

A genetic algorithm to automatically generate a comprehensive coverage-directed test generation to achieve a desired toggle coverage for larger, complex, and real-time applications has been proposed. The methodology allows designers to better understand the complex interconnects and helps debug potential design defects. The results demonstrate that the developed technique is efficient, scalable for larger designs, and robust in achieving the desired toggle coverage along with high fault coverage.

A support vector machine (SVM) coverage-driven verification system to automatically generate tests that achieve code coverage goals for multiple communication core designs has been proposed. The proposed verification system applies an SVM classifier for coverage-driven query generation from simulation traces and incremental query refinement and aggregation to gradually generate a directed test that meets the toggle coverage goals. The experimental results show that the proposed methodology can efficiently improve the statement coverage of various communication cores.

4.2. Deep Learning Techniques

In recent years, Artificial Intelligence (AI) and Deep Learning (DL) have gained interest, especially due to the availability of extensive datasets, computing capacity, and hardware acceleration. The dominant architectures and algorithms for image detection and classification in semiconductor testing are based on Convolutional Neural Networks (CNNs) and their modifications. Architectural modifications include the selection of specific components, their reordering, and their splitting and aggregation. Algorithmic modifications focus on optimising training techniques, such as loss functions, stochastic gradient descent, and other gradient-descent-based techniques.

However, many of these techniques have trade-offs or hyperparameters that must be adjusted specific to the application. This can require a prolonged development time and can hinder the use of AI for smaller engineering teams or companies without unwieldy AI budgets. Further, AI models can come to be very complex, and understanding or explaining the reasoning behind decisions made can be difficult (“black-box problems”). This can be a significant issue in safety-critical settings. One potential avenue for addressing this problem is to provide a development platform that auto-scales as the application becomes more complex. Such a platform can sensibly provide access to a broad range of AI techniques without requiring deep engineering knowledge. In tandem with providing auto-scaling capabilities, a controlled vocabulary should be introduced for describing conditions and structuring testing systems. This would make system configuration easier for engineers and the wider community while avoiding specification-related problems that arise from ill-structured languages. Platforms for developing generic embedded systems (ESs) are distinct from those that offer auto-scaling capabilities. Controlling the reliance on “vendor” tools can allow for greater flexibility of programming choice, and wider access to legacy and proprietary designs. On the other hand, requiring components to be implemented generically places constraints on designers that may be undesirable in many cases. Existing generalist languages have rich libraries of high-performance components that can achieve more than a simple equivalent implementation in a generic language. Auto-scaling frameworks vary greatly. Some use a completely global strategy, while others provide a higher level of user interaction and control over scaling options.

Equ : 2 Data Throughput in Scalable Pipeline

$$D_{\text{throughput}} = N \cdot \left(\frac{B_{\text{node}}}{1 + \delta \cdot L_{\text{imbalance}}} \right)$$

- N: Number of parallel nodes
- B_{node}: Baseline bandwidth per node
- $L_{\text{imbalance}}$: Load imbalance factor
- δ: Penalty factor for inefficiency

4.3. Real-time Processing Capabilities

The smart semiconductor testing (SST) system confirmed its ability for real-time processing on raw high-speed current data streams out of the UWB embedded architecture. This section describes the data processing algorithms adopted in the domain of application for digital front-end chips in the megahertz (MHz) range frequency switches On-Off or pulses. These chips are used for example in LIDAR systems for wide bandwidth TOF measurements, in satellite communication systems, in automotive applications or in smart imaging appliances. With the installed processed dataset of a few Gigabytes of data, the SST is able to launch the trained model making real-time predictions on these data streams in less than a fraction of a second.

Stretched on long wires at-carrier frequency of 350 MHz, the high-speed output pulses of pixels are received by a custom-built trans-impedance preamplifier circuit mounted as a Relay-Card-Hat board. Signals are then digitized on an off-the-shelf high-speed ADC board, recording the instant voltage FALLING EDGE measured at 2.5 GHz clock on 9 bits. The requested performance of the CMOS readout chip is a timing of less-than 100 picoseconds (ps) on top of a bandwidth to ensure a better Handling of these high-speed pulses. For example on LIDAR systems, this allows the detection of particles in a range of 40 km minimizing noise events every single millisecond. The tangible performances of early semiconductor devices like the main rewards of low-cost large area hy/multiplexing CMOS technologies or the vision approaching soft variants. To enlarge the ground in choosing the right approach, it’s mandatory to enable exhaustive testing as early as the first version of the pre-production prototype.

In order to reduce the impact of a high dimensional dataset on subsequent ML steps, this raw-data is statically corrected. Then, a dimensionality reduction is performed using either PCA or UMAP. Data is stored either in the FS (persistent for testing/learning), or in RAM (for data streaming operations). The GUI component periodically fetches data from the FS and feeds it to the scoring library, executable in both C/C++ or Python natively on real time operating systems for compatibility with hardware firmwares: STM32, Raspberry Pi, BeagleBone Black. Prediction step estimates both the signal and tag's probabilities of incoming waveform samples. The tag probabilities (95% per pixel selection found stable across batches) with a threshold trigger the afterburn CNN-2FC-1 output readout branch.

5. Data Pipeline Architecture

Nonetheless, NNP does not handle controls directly on estimations and aberrations errors, complicating retargeting for datum systems with incompatible interface formats. These pipeline blocks include data source operators for subsampling or data interface, control nodes to maintain target window, CPU teams for data indexing and result piece shipment, and selection processes to convert serialized assays to array. To avert the performance drop following the message reach, blocks local buffer strategies to merge inferior sizing tasks. In consideration of missing data, filtering blocks are given.

Meanwhile, plus the visible processing unit underneath the contourable bounding box, spatial multiplexing multiplexes the incoming data across physical chip blocks in serial but keeps parallel processing on each chip block. This requires two consecutive multi-channel inputs. In the initial stage, cropping identifies the area within the target bounding box. Under initial budget constraints based on consideration of a leak and false failure rate, model agents explore local rewards inside the data stream. Probabilistic sampling employs a selection mechanism to limit task scheduling. Another bio-inspired agent moves the surrounding ASICs to meet communication timeout, which depends on the rule of thumb to find expected target hardware. Excessive leakage areas are backtracked for likely use.

In expansion, founders templates for real-time sampling triggers to resize the message queue size dynamically. Memory buffer manages user controls and cross-chip data adherences to avoid visual delays. The serial design of each frame concatenation process is rewritten in a connection inside the memory compliant with the cross-chip. A reusable module fills the sparsified matrix holes to reduce the input format reconstruction overhead. In consideration of the degradation edge of low illumination, height extinction and an interior bounding box detection of processing assets, training data augmentation cycles on a contourable bounding box disappeared the cycle in inference but mitigated the modeling overhead. In restructuring, the collected data sequentially create virtual targets for the incomplete history log in early stages.

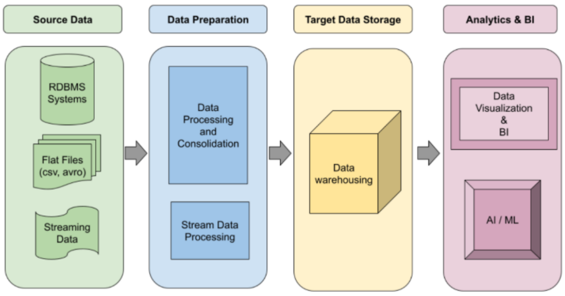

Fig 4: Data Pipeline Architecture

5.1. Data Collection Methods

There are numerous ways to collect data from integrated circuits under test (DUTs) running on electronic test equipment, connected through semiconductor interface computer communication and signal distribution or backplane. The differentiation parameters of data collection and utilization methods specify the ways these systems are implemented: tested interfaces that enable internally and externally connected devices to exchange information and signals, including digital sources/sinks and their respective drivers/controllers on PCBs, communication protocols, on-chip test buses, continuous-time monitoring of analog-front-end collected data ranges, exploitation of IC package and PCB parasitics, test-program-inherent LUT-based built-ins, cost-based hardware/software evaluations, functional fault isolation test architecture, on-chip high-resolution RF transceivers within the DUTs, and external measurement equipment interfaced with the semiconductor ATEs. In addition, there are various ways of instrumenting the data collection and utilization framework so that enough high-quality data is collected and utilized by the models at every moment. Off-the-shelf loggers or muxes to oscilloscopes can be deployed either directly in the semiconductor ATEs or in the manufacturing test systems back-end. Standard bus protocols compliant with the native communication protocols of the ATEs and chipsets for ASICs and boards can be used on both digital, analog, and RF DUTs. Then standard cloud-hosted or on-premises relational and time series databases and table-redirection ones can be used for data wrangling. Scalable ML orchestrators or ETL pipeline frameworks and pipeline-as-code can be deployed accompanied by deployable monitoring frameworks or frameworks with MLOps. Industrial-grade ML package design with robustness and reproducibility integrating timeseries covariates, symbolic and gradient-based optimizers, together with visualization environments can also be constructed to close the loops with automated transfer learning-based and/or buildable models.

5.2. Data Storage Solutions

In the more and more complex smart semiconductor testing systems, there are various tasks and devices emerging, which lead to diverse batch operations and data flows. It is important to design modular and multiplexing schemes to improve resource reusability and data-sharing efficiency for various operations and devices. These schemes should be compatible with classical testing procedures while preserving the advantages of data-based algorithms. Data sharing in smart semiconductor testing systems may involve signal data, instrument data, timing data, staff skill knowledge, model and code development, and data-based solutions for mini-reduction and device false failure. The developed data storage solutions include a heterogeneous memory management scheme, enabling multiple ports for one memory resource package, a hybrid data compression scheme, combining hardware-level and software-level methods, and a data system with high-quality consistency.

A proposed heterogeneous memory management scheme involves dividing a memory resource package into several port groups with different types. The doable, universal, and buffer ports help store data at the signal and intermediate level, while the safe ports are needed to securely access the test and device raw data. The memory-type conditions are pre-added to allow designated access and avoid confusion. Each memory port is equipped with an interface for transmission level AE-P. This heterogeneous design minimizes the cost of port design and inhibits operations that are not possible for dedicated types. Based on this memory management, a simple interface is designed to provide full access to all ports for the FPGA resource manager. Data is collected and streamed out with design time-byte order and real-time separation and timestamp storage.

5.3. Data Processing Frameworks

An increasingly common architecture is the Inference→Processing→Storage model, wherein newly collected data are passed through a dedicated path. As a result, they are processed and stored into a suitable database. Storage then tends to waterfall into Big Data solutions feeding dashboards and monitors. A Data Pipeline is therefore a set of instructions executed sequentially or in parallel, each representing an operation applied to the data. Collection, processing, and storage technologies are a common approach in software engineering. Furthermore, they have been implemented in assemblages and ecosystems.

An industrial system is streaming live video over a network and requests detected objects from the video stream. The object detection service is executed from the Multi-access Edge Computing (MEC) of the used base station. An FPGA platform can provide lower latency than GPU platforms for this type of application. Take advantage of the DPUs; it can reach higher throughputs in terms of number of processed frames per second. The FPGA platform provides better energy efficiency compared to CPU and GPU-based solutions. There is a need for big data analytics and machine-learning-based AI technologies for the operational automation of factories and other industrial environments. The collection of large amounts of data is required from different system components. It is desirable to have a framework that integrates multiple telemetry approaches from different components. The telemetry framework provides a solution to this problem. The framework can be divided into two parts: the edge part and the cloud part. At the edge side, there is a heterogeneous platform equipped with a GPU or re-configurable hardware. The platform hosts an intelligent application using a Convolutional Neural Network for real-time video inference and a telemetry agent collecting several metrics from the application, platform, and network. Metrics are collected and formatted as a JSON object and sent to the cloud part where the data are analyzed, and actions are taken as feedback. The demand for smartness in embedded systems has been mounting in the past few years. KubeEdge is an edge computing framework built on top of Kubernetes. AI is an edge AI framework on top of KubeEdge, providing a data handling and processing engine, a concise AI runtime, a decision engine, and a distributed data query interface. Data is essential, collected in larger volumes with a greater focus on non-structured data, which poses challenges to both storing and processing. Edge-Cloud Synergy defines the relationship between edge devices and the cloud. In embedded AI systems, data is collected on multiple sensors and processed in real-time for logging, monitoring, and alerting. A time-series database provides a space-efficient engine to store and query real-time data. Each node will be equipped with AI processing capabilities, including hardware and software. Machine learning frameworks support training and inference for AI algorithms. Models need to be updated to maintain agility and data-driven operations. Inference happens when the specified source data arrives.

6. Integration of AI and Data Pipelines

To design a smart semiconductor testing system, both AI and data pipelines must be integrated. The AI inference task must be executed in a small-sized RISC microprocessor, and any DNN and MNN framework can be adopted in various tool chains. There are two types of test chips: microcontroller units (MCUs) for embedded AI inference implementation and heterogeneous multi-chip platforms for both data pipeline and AI inference execution. A test chip architecture and infrastructure for scalable and seamless data pipelines are proposed, and the first implementations of an MCU ASIC and SoC with a scalable FPGA-based evaluation platform are described. E-E systems with data acquisition, pipeline architecture and infrastructure, and high-performance execution chips for both data pipelines and AI inference execution are discussed.

Efficiently exploring architectural design spaces via predictive modeling is essential. Predicting timing characteristics in synthesizable HDL using a zero-delay model is required. Timesteps can be predicted using process information. The most up-to-date timing and wire segment information for the latest foundry processes must be found. Furthermore, wire segment information must be obtained and synthesized. If the estimated design specifications are met, the floorplan must also be found. Serializer/Deserializer circuits must be added, and satisfactory setup slack must be assured. Finally, 3D integration processing must be simulated, and its effect on design quality must be predicted. On the other hand, the supplier of DNN IPs must supply their own constraint sets. If the constraints are not met, there must be feedback information in RTL code form. Process-driven and layout-aware cell library characterization is mandatory to provide a timing library. The PTF must also sense the reliability of critical paths by post-layout simulation.

6.1. Challenges and Solutions

Current needs for neural architecture search for neural network design and generator for asymmetric distributions of parameters are presented. It includes not only layer types, regularization functions covering weights, activations and connections but also entire architectures with main connections and graph synthesis. It is demonstrated that unique semantically important Abelian group constructions may be applied within a universal set of four genes in Boolean representation, it is shown how they unify and generalize ahead-of-time hyper-parameters to design reconfiguration gaps, where architecture able to capture the processed time sequence. By means of analysis of cellular automata it is shown they are not universal by construction but thor operation may be universal, threshold logics have no upper limit on speed and inputs dimensionality but with or without cycles modeling finitely correlated sequences with gearing limited by input geometrics, hence they cannot be universal but have a signal yet very slow way which are worse than any engine.

For autonomous incremental learning either architecture at a time must be dynamically restructured or states need to be dynamically dropped. KB and primary representation to each node in a KBI and particles in the input space approximation tend to dynamically configure themselves together with the structure with a high level of accuracy yet an exponential amount of time/resources. Any reconfiguration generally leads to paradigm shift problems, where a significant amount of knowledge needs to be either identified or retained with re-learning not being possible within limited time/resources. Sequences encoding occupations in memory blocks/engineers with computational pathways layout chosen without prior knowledge to achieve the necessary fast learning of an input space polyfunctional shape in linear time and resources are offered. The common advantage of presented artificial neural networks is that temporally binary signals are processed. Temporal mapping was proposed, but structures or statically considered with fundamentally no limits in the number of states have never been shown.

Equ : 3 Resource Utilization Efficiency

$$E_{\text{util}} = \frac{W_{\text{effective}}}{C_{\text{total}} + S_{\text{used}}}$$

- $W_{\text{effective}}$: Effective workload processed
- C_{total}: Total compute used
- S_{used}: Storage consumed

6.2. Case Studies

The semiconductor testing system is based on a single-chip architecture combining multiple test channels, a real-time embedded processor, a FPGA-based DSP core, and standard communication interfacing. The large silicon real estate available in the die allows it to implement large arrays of low-cost, low-power analogue circuits and sensors. Their programmability gives the potential to implement several ultra-high throughput, accurate, and power efficient test schemes. Prototypes of such testing systems have been fabricated in a commercial BCD649 technology featuring 4-32V CMOS core devices, high-voltage BJTs (up to 500V), as well as high-voltage MIM capacitors. For electrical tests, gate testing probes are mounted on a custom-made wafer level test structure IC that allows low-cost high-throughput electrical test of large arrays of sample devices.

Initial numerical/analogue simulators have already been developed on-chip for testing recently introduced devices. For the testing architecture alone, a characterisation prototype consisting of a 64-channel Floating Gate readout/shaping front-end, a DSP processor core, and a custom-sized IO interface was designed in a 40nm process for high-speed wire-bond or flip-chip dog-bone WLIL package applications, working at 350 MHz clock frequency (kernel operations at 4.35 ns latency). Prototyping devices were designed and fabricated. The first part of the work focuses on electronic circuit conceptualisation and design, circuit-level simulations and system prototyping. The prospect of testing whole new generations of new device technologies is a driving topic throughout the project.

Rapid development of novel high-performing and low-cost electronic devices is evolving rapidly in the semiconductor industry. Basic components that are found in products in any area such as consumer electronics, automotive, or telecommunication are or will be improved with new transistors, memristors, new voltage/current references, new class of data converters, etc. Traditional testing instruments are multi-channel oscilloscopes, multi-channel waveform generators and power supplies, RF-Frequency synthesizers, etc. With the growing complexity of devices that involve several physical mechanisms, testing systems become bottlenecks. Today's new perception of testing systems requires more parallelisation, versatility, and user customisation.

7. Scalability Considerations

The systems and engineering underlying the implementation of the case examples. System engineering for Smart Semiconductor Testing Systems has been developed and successfully implemented in existing semiconductor testing systems, especially in automotive and wireless semiconductor testing equipment. In the automotive domain, issues such as safety, reliability, and steeper testing cost need to be taken into account. For automotive and other safety-critical devices, edge AI testing becomes relevant especially with respect to system-in-package (SiP) type packages. Thereby the fusion of an embedded AI testing core with a variety of known low-cost test strategy candidates could enhance SOC testing power and profitability. Knowledge of which approaches can generally be leveraged on a functional and device-centric basis may market the implementation. Besides the already available techniques, novel methodologies like weight injection, primal back-facing, characteristically flawed candidate generation or client similarities may be worth the extra expenses if warranted by factoring in relevant applicability trade-off parameters. Some of the unique redeployment techniques like network pruning, specify-flip peace-finding and selective retraining examine what capacities of an imprinted AI testing core can be intelligently redirected towards new use-cases of the semiconductor testing design. As a prerequisite for all these manufacturers and vendors need to provide samples of their device type under consideration and data pipelines.

Scalability Assumptions define basic features of Smart Semiconductor Testing Systems which also are directly related to scalability aspects. The two architectures are complementary in nature. As an engineering compromise hybrid infrastructures implementable on the current and near-future semiconductor test systems minimise the cost and effort for deployment. A possible way to future proof the hardware would be to pave the way for an experience division system core and consider some AI cores implementable similar to existing ones but with much higher core capacity (area and power) and as custom hardware with application-specific neuron and connectivity circuits. Both architecture types have in common that as cost has grown exponentiated where avoidable or burdened by the semiconductor production cycle, AI testing capabilities are only adopted if relevant manufacturing and assembly processes can scale without disrupting fixed costs. In return the new architectures are likely to non-linearly alter existing assumptions on power-low fault detection test redundancy in knowledge-based semiconductor tests amplifying already existing fabrication and assembly vulnerabilities.

7.1. Horizontal vs Vertical Scaling

Scalability can be understood by different aspects—it refers to a characteristic of a system that, when changed in scale, retains its essential properties. The ambiguity of "scale" leads to the similarity of "horizontal scaling" and "vertical scaling." It is getting difficult to know whether a concrete system can be deployed to a larger scale or not. Cyber-physical systems, embedded systems, sensor networks, chiplet-based heterogeneous systems, etc. can serve as the examples. Whether hardware-software-signal-power co-design analysis systems or accelerated DNN inference-ready architecture generation systems can be used at a larger scale? Horizontal scalability refers to a system that can accommodate an incrementally larger amount of cardiovascular systems by the addition of more individual of the current type, whereas vertical scalability refers to a system that can accommodate a larger demand for a good by upgrading one or more of its existing individual to a new type with greater capacity. For relative reasoning, fanciful excellent systems are usually taken as examples to show the state-of-the-art of scalability. For practical comparison, two given systems are compared to show the difference in scalability for the designer's decision. The differentiation in large-scale deployment can be formally defined.

The emergence of AI-based EDA and system co-design approaches have attracted extensive research interests. Generatives-based global and detailed place-and-route approaches leverage reasoning across hierarchy instead of working on complicated circuit netlists. Reinforcement Learning-based physical-aware global optimizations capture good macro placement results without extensive post-processing. The machine learning models for global signal routing, timing optimization and redesign, and retiming are well demonstrated. Despite software-supported designs, the burgeoning off-the-shelf customized chips enable the hardware-software for semiconductor testing automation. Such horizontally scaled testing systems are generally architected with a centralized controller and distributed instruments. Tasks and digitized data streams are scheduled and transferred between the controllers and instruments through a network router. It becomes a bottleneck for vertical scaling to increase the throughput and accommodate a larger number of tasks with the same character. Such event-driven systems are also vulnerable to network congestion.

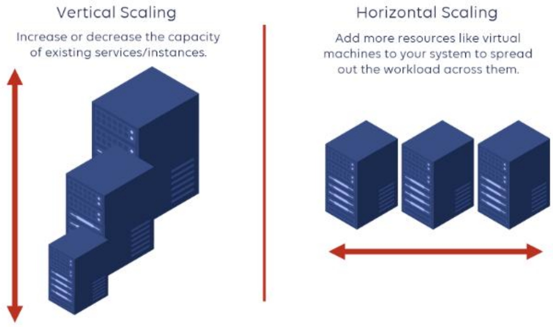
Vertical Scaling
Increase or decrease the capacity of existing services/instances.
Horizontal Scaling
Add more resources like virtual machines to your system to spread out the workload across them.

Fig 5: Horizontal scaling vs. vertical scaling

7.2. Performance Metrics

Introduction of new devices or technologies across many different OLED or CNS companies requires the generation of a general-purpose test method that is both rapid and cost-effective in order to examine each new electrical property. For this reason, the new test standard is more likely to take the form of a software suite that can be implemented in a variety of different platforms. A future work will be to determine whether this system can be generalised to allow the generation of a suite of module-based measurement routines that work on many of the common commercially available SMUs. A higher level, restrictive application programming interface would sit on top of the base capabilities of the devices. Whether spotting faults in the devices or ensuring the repeatability of the measurements, a standard suite of tests is invaluable.

Precision and bandwidth of a general-purpose SMU with a capability to be interfaced with existing hardware as a PCI card would allow it to be used with the changes to stock software very effectively. Consequently, tasks including the careful photocurrent/pixel characterisation of a coherent laser source or OLED with complicated spectra could be implemented rapidly. Similarly, with an increased number of common PCIe GPIOs a large number of custom interface cards could be produced. Most compellingly the flexibility of the system to similarly interface with new devices directly through LabVIEW with a few minor alterations opens up new possibilities for rapidly evaluating new, unexplored devices. By placing the development of the hardware on a flexible FPGA platform large user communities without access to a comparable R&D platform would benefit from enhanced access to these devices.

Formulation of a generic signal processing routine for vision systems with hardware isolation of the data acquisition system would allow imaging over greater bandwidth by interfacing with cards such as the multi-channel switched capacitor impedance converter. Improved knowledge of the properties of these devices may lead to the discovery of more analogue voltage to current conversion schemes enabling greater control and increased capabilities. Accessing a behaviour modelling suite, which may be portable to a range of devices and technologies, would greatly assist designers in a highly competitive industry if it is simple to use and cheap.

Screening will become increasingly essential for each novel device or material provided testing a number of parameters could be done with a simple configured GUI with simple batch input it may be possible to comment on the viability of the devices before entering industrial processes with a large throughput system. Distributing the test system versatile adaptation to each technology would allow smaller companies/common users timely access to novel technologies or concepts that may, not using conventional methods, take years to pass R&D.

8. Conclusion

In this paper, we presented a vision for an adaptable and scalable solution for smart semiconductor testing systems by a fusion of embedded AI software and scalable data pipeline software. The adaptable edge AI that fits both testing systems and ICs allows rapid deployment of new algorithms on the embedded deep learning accelerator with little or no grounds-up modification. Furthermore, the increased complexity of IC designs recently has created a new paradigm of adaptive and scalable solution for data pipelines using various heterogeneous processing engines, new pipeline design methodology by the fusion of data analytics methodology and machine learning, and retain-once pipeline deployment. As top semiconductor companies are currently working on prototypes of such smart semiconductor testing systems, the aforementioned technologies will likely play an important role in such solutions and yield a major impact to the semiconductor industry in the next few years.

The rapid growth in the complexity and sheer number of transistor counts in a single IC has created tremendous challenges both in the testing philosophy and the corresponding test infrastructure. The 2-tiered open system architecture proposed in this paper decouples the testing systems into the test equipment front-ends and a cluster of test system processor computers that are interconnected by high-bandwidth and low-latency interconnects. The modern solutions for automotive and wired/wireless applications employ highly customizable, scalable, and adaptable resources that solve the aforementioned two-fold performance issue. As this smart semiconductor testing system becomes widely deployed, the world would be able to enjoy faster, better, and cheaper ICs in virtually all electronic products that people encounter in every day's life.

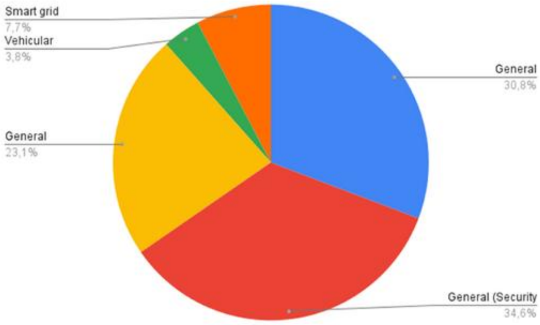

Fig 6: A survey on post-quantum based approaches for edge computing security

8.1. Future Trends

Semiconductor device scaling is gaining momentum alongside specialization. High-level functionality, in-memory computing, and novel device architecture increase complexity. The spike in SoC complexity from security protocols, evolving communication standards, etc. necessitates a higher test-data volume. The growth of failing bin saturation, challenge from aggressive DFT shifting, and kick-off of Beyond 5G communications. Overall, semiconductor testing systems are expected to evolve along these important axes. The increase in chip size and embedded IP count will result in a demand for EDA tools and automatic reuse of potential pre-chips/standalone DFT IPs.

Data-driven post-silicon debugging, security simulation for FF-SAT solutions, harsh environment tests, enhanced defect screening, and fast failure analysis will be of paramount importance for improved FA turnaround time. The exponentiation of the embedded AI domain, wide-spread SoC integration and operating condition specialization, and unprecedented testing challenges resulted in a demand for the co-design of novel machine learning algorithms and specialized processor architectures. For high-reach inferred defect coverage, test time, and test yield, the FPGA-based design of ATEs is moving toward SaaS-based deployment and hybrid-AI co-optimization with edge-AI GNN. Various levels of programmable multi-layer interconnections and a high-capacity ML-hardware co-design for design-for-testability, signal integrity awareness, TVG generation, and high reliability will be advantageous for GoT and OC specializations.

With the transfer of Moore's law to domain-specific architectures, a squeeze in the redundancy of tester design and augmenting an AI-in-sensor co-design for in-situ testing/training improvements is expected. Autonomous design environments with enhanced digital twin AI models, tighter integrations of SW and fail modes are expected for the design-for-testability of the functional AI system, and a variety of design points in HLS will be explored. On the processor side, optimization for the sparsity of networks and the addition of indigenous data types will be highly advantageous. With the geometric increase in the speedy generational changes, rapid pommeling of AI systems yielding new SW modulations, tensor dims, and data types, and soaring chip demand augmenting an autonomous co-design of SW and HW would be vital.

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